UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/980,098	03/15/2002	Shinji Itami	Q67475	1120

7590 06/08/2005

Sughrue Mion
2100 Pennsylvania Avenue NW
Washington, DC 20037-3213

EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,098	ITAMI, SHINJI	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6,8 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 4th of April 2005 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/980,098, which the request is acceptable and an RCE has been established. Claims 1, 5, 6, 8 and 10 have been amended; no claim has been canceled; and claim 10 has been newly added since the Final Office Action was mailed on 3rd of December 2004. Currently, claims 1, 3, 5, 6, 8 and 10 are pending in this application.

Examiner's Notice

2. The Amendment document in the Response is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121, as amended on June 30, 2003 (*See 68 Fed. Reg. 38611*, Jun. 30, 2003). See MPEP 714 [R-2] and 37 CFR 1.121(c).

In fact, the claim status of the claim 1 is not (previously presented), but (currently amended), and the claim status of the claim 10 is not (previously presented), but (new), because the Amendment after final was not entered (See Advisory Action, item 3, mailed on 15th of March 2005, paper no. 20050311) into a record.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5, 6 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

In fact, the claims 5, 6 and 8 recite the limitation "said address is not incremented when a waveform is deformed by said trigger signal" in lines 20-21 of the claim 5, in lines 17-18 of the claim 6, and in line 19 of the claim 8, respectively. However, the claimed limitation was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5, 6 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 5, 6 and 8 recite the limitation "the second board" in line 22 of the claim 5, in line 19 of the claim 6, and in line 21 of the claim 8, respectively. There is insufficient antecedent basis for this limitation in the claims 5, 6 and 8, respectively. Therefore, the Examiner presumes the term "the second board" could be considered as --the secondary board-- since it is not clearly defined in the claims.

The claims 6 and 8 recite the subject matter "the address" in line 17 of the claim 5, and in line 19 of the claim 8, respectively. However, the claims recite "the start address" and "the incremented address" as an antecedent basis for this subject matter, respectively, which does not particularly point out and distinctly claim the subject matter which applicant regards as the invention. Therefore, the Examiner presumes the term "the address" could be considered as --the incremented address-- because of the above mentioned reason.

The claim 6 fails to positively recite the boundaries sought for protection. The metes and bounds of the claim cannot be determined because it is unclear as to which category of subject matter is sought for protection, i.e., the method or the apparatus. In other words, the claim language does not adequately specify what is covered in its metes and bounds should it mature into a patent. It is essential that the

Applicant makes clear what is covered by the claim in order to determine patentability. See *In re Steele, 49 CCPA 1295, 134 USPQ 292.*

In this case, the claim 6 recites a process of use, i.e., carrying out data transmission using data transmission system, in the apparatus claim, i.e., data transmission system.

Therefore, the Examiner presumes that the Applicant seeks for protection of the apparatus claim in order to make clear what is covered by the claim, and rejects the claim based on a prior art in the category of subject matter being sought for protection.

The claim 8 recites the subject matter "the data transmission/reception" in line 7. There is insufficient antecedent basis for this subject matter in the claim. Therefore, the Examiner presumes the term "the data transmission/reception" could be considered as --the data write-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1, 3, 5, 6, 8 and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art [hereinafter AAPA].

Referring to claim 1, AAPA discloses a data transmission system (Fig. 16), comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) carrying out data transmission/reception (See page 1, lines 16-20) between said primary board (i.e., said primary

board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side),

- o said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15), wherein
  - ▪ when said data access (i.e., Reading Process in Fig. 20) is executed from said primary board to said secondary boards (See Figs. 20 and 21), informing a start address (i.e., Step S211- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 20) required for data access (See page 3, line 24 through page 4, line 4), and wherein
    - • an address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) used in said data access (i.e., accessing DATA 1-4 in Fig. 19) in said secondary boards (i.e., said DATA 1-4 are in said secondary boards being addressed by said generated address; See page 4, lines 8-21) is generated based on said start address (i.e., said A15:2/D 15:0 START ADDRESS OUTPUT), a predetermined trigger signal (i.e., trigger signal TRG 201 in Figs. 17 and 19) and a cycle signal (i.e., signal A1:0 in Figs. 19 and 20) indicating switching of data (See page 5, lines 6-18), said cycle signal is combined with said trigger signal (i.e., said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 4, line 22 through page 5, line 18).

Referring to claim 3, AAPA teaches

- when said address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) is generated based on said trigger signal (i.e., trigger signal TRG 201 in Figs. 17 and 19; See page 4, line 22 through page 5, line 5), said address is generated sequentially by incrementing said start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19) in response to a timing of said trigger signal (See trigger signal TRG201 and signal A1:0 (205) in Figs. 17 and 19, and page 5, lines 6-18).

Referring to claim 5, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data transmission/reception (See page 1, lines 16-20) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side), where
    - said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15), wherein:
        - when said data access (i.e., Reading Process in Fig. 20) is executed from said primary board to said secondary boards (See Figs. 20 and 21),
            - informing a memory start address (i.e., Step S211- A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 20) of said secondary boards required for data access (See page 3, line 24 through page 4, line 4),

- judging in said secondary boards is performing whether or not said memory start address is directed to own station (See page 2, line 25 through page 3, line 3; i.e., Separator 207 in Secondary Board 200 in Fig. 17 is performing the step S201 in Fig. 18), and then
- executing said data transmission via said data transmission path (i.e., data transmission bus) by accessing a memory (i.e., Memory 208 of Fig. 17) in own station (i.e., target Secondary Board 200 of Fig. 17) based on said memory start address when said memory start address is directed to own station (See page 3, lines 4-13 and Fig. 18), and

o an address (i.e., a generated address based on Start Address A15:2 with signal A1:0 in Fig. 20) is generated, to which said data transmission is subsequently executed (i.e., steps of S214-S220 in Fig. 20), in said secondary boards (i.e., address is constructed in said secondary boards by synthesizing the address A15:2/D15:0 assigned from said primary board; See page 4, line24 through page 5, line 2) by

- incrementing said memory start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19) after said data transmission based on said memory start address is ended (i.e., steps of S211 and S212 in Fig. 20), and then
- executing said data transmission via said data transmission path by accessing said memory of own station (i.e., target Secondary Board) based on said generated address (See timing diagram in Fig. 19 and page 5, lines 6-18), wherein
  - a cycle signal (i.e., signal A1:0 in Fig. 20) indicating switching of data (See page 5, lines 6-18) is used in combination with a trigger signal (i.e., said secondary board interprets said signal A1:0 and trigger signal TRG

201 in Figs. 17 and 19 as combined for outputting said DATA 1-4; See page 4, line 22 through page 5, line 18), wherein

- said address is not incremented when a waveform is deformed by said trigger signal (See Fig. 21, in fact, an address generation at Step S233 is not repeated (i.e., going to End of Reading Process at Step S232) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data accessing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that said address is not incremented when a waveform is deformed by said trigger signal. In other words, a synthesized address construction, which is based on Start Address A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data accessing process by a noise from trigger signal TRG 201, for example, in Fig. 19), and wherein
- said secondary board does not shift to a next process until a phase has been toggled (See page 4, lines 8-21; i.e., the secondary board does not proceed to the next process S234 Memory Read in Fig. 21 until the bus direction has been changed from input to output, and the cycle has been switched from the address cycle to the data reading cycle) and leading and trailing edges of said trigger signal are detected in combination with detecting said toggle states of said phase (See page 4, line 15 through page 5, line 3).

Referring to claim 6, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data read (See page 1, lines 16-20 and page 3, lines 14+) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side), wherein
    - said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 19 and page 2, lines 11-15).

Referring to claim 8, AAPA discloses a data transmission system (Fig. 16) comprising:

- a primary board (i.e., primary board 100 of Fig. 16);
- secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16); and
- a data transmission path (i.e., data transmission bus 300 of Fig. 16) for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between said primary board (i.e., said primary board on the transmission transmitter side) and said secondary boards (i.e., said secondary boards on the transmission receiver side), wherein
    - said data transmission path (i.e., said data transmission bus) employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 22) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 22 and page 2, lines 11-15), wherein said carrying out of said data write (i.e., --Writing Process-- on page 5) is executed by:

- informing a trigger signal (i.e., trigger signal TRG 201 in Figs. 17 and 22) combined with a cycle signal (i.e., signal A1:0 in Fig. 22; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 6, lines 17-24) indicating a timing of data access (See page 6, line 25 through page 7, line 11) and a start address (i.e., Step S241- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via said data transmission path (i.e., data transmission bus),
- switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17);
- accessing said memory (i.e., Memory) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and Steps of S241 and S242 in Fig. 23), and then writing said predetermined data to be written into said memory (See page 6, lines 6-16),
- incrementing said start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 22), and then writing sequentially said predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via said data transmission path (i.e., Data Bus), into said memory by accessing said memory based on said incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6),
- detecting leading and trailing edges of said trigger signal in combination with detecting toggle states of a phase (i.e., detecting TRG with detecting toggle states

of Addressing cycle phase and Data cycle phase in Fig. 22; See page 6, line 17 through page 7, line 1),

- not incrementing said address when a waveform is deformed by said trigger signal (See Fig. 24, in fact, an address generation at Step S262 is not repeated (i.e., going to End of Writing Process at Step S261) for address increment when a waveform of FRAME is not L (i.e., Low) caused by signal deformation to H (i.e., High) in the middle of data writing process by trigger signal TRG, e.g., a noisy trigger signal, inherently anticipates that said address is not incremented when a waveform is deformed by said trigger signal. In other words, a synthesized address construction, which is based on Start Address A15:2/D15:0 (206) with signal A1:0 (205), is not repeated, viz., no address increment, when a waveform of FRAME 202 is deformed to H (i.e., High) in the middle of data writing process by a noise from trigger signal TRG 201, for example, in Fig. 22), and
- not shifting said secondary board to a next process until said phase has been toggled (See page 6, lines 15-24; i.e., the secondary board does not proceed to the next process S264 Memory Write in Fig. 24 until the cycle has been switched from the address cycle to the data reading cycle).

Referring to claim 10, AAPA discloses a method for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A15:2/D15:0 206 of Figs. 17 and 22) as an address bus (i.e., Address 15:2)

and a data bus (i.e., Data 15:0) mutually (See timing diagram for A15:2/D15:0 206 of Fig. 22 and page 2, lines 11-15), comprising:

- informing a trigger signal (i.e., trigger signal TRG 201 in Figs. 17 and 22) combined with a cycle signal (i.e., signal A1:0 in Fig. 22; in fact, said secondary board interprets said signal A1:0 and said trigger signal TRG as combined for outputting said DATA 1-4; See page 6, lines 17-24) indicating a timing of data access (See page 6, line 25 through page 7, line 11) and a start address (i.e., Step S241- A15:2/D15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via said data transmission path (i.e., data transmission bus);
- switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17);
- accessing said memory (i.e., Memory) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and Steps of S241 and S242 in Fig. 23), and then writing said predetermined data to be written into said memory (See page 6, lines 6-16);
- incrementing said start address (i.e., said Start Address being incremented with A1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 22), and then writing sequentially said predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via said data transmission path (i.e., Data Bus), into said memory by accessing said memory based on said incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6).

Response to Arguments

9. Applicant's arguments filed on 24th of September 2004 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... Specifically, claims 5, 6, and 8 are related to a technique to prevent malfunction of a multiplexer due to disturbance of a signal (trigger signal). The address is not changed only by the variation of the trigger signal, but is changed using the cycle signal in combination with the trigger signal. Therefore, the object of the present invention is different from that of Oshikawa, ..." on the Response page 8, this argument is moot in view of the new ground(s) of rejection.

However, the reference AAPA in the prior art of the record inherently anticipates the above argued elements (See paragraph 8 of the instant Office Action, claims 1, 3, 5, 6, 8 and 10 rejection under 35 U.S.C. 102(a) as being anticipated by AAPA).

Furthermore, the amended claims are failing to comply with the written description requirement under 35 U.S.C. 112, first paragraph (See paragraph 4 of the instant Office Action). In fact, the amended claims 5, 6 and 8 respectively contain subject matter "said address is not incremented when a waveform is deformed by said trigger signal" which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Therefore, the Applicant's argument on this point is not persuasive, as well.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takahashi [US 6,212,615 B1] discloses semiconductor circuit having burst counter circuit which is reduced the circuits passing from the clock input terminal to output terminal.

Awamoto et al. [US 4,757,392] disclose error compensation by a ramp waveform having a high signal-to-noise ratio.

Kojima [US 4,588,905] discloses digital waveform conditioning circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 5:30am - 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/ cel